

**Amendment and Response**

Serial No.: 09/603,132

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For: DEVICE STRUCTURES INCLUDING RUTHENIUM SILICIDE DIFFUSION BARRIER LAYERS  
(As Amended)

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B2  
30. (Once Amended) The structure of claim 27, wherein the at least a portion of the surface is a silicon containing surface and further wherein the structure includes one or more additional conductive layers over the diffusion barrier layer formed of at least one of a metal and a conductive metal oxide.

B3 SW D2  
32. (Once Amended) A capacitor structure comprising:  
a first electrode;  
a high dielectric material on at least a portion of the first electrode; and  
a second electrode on the dielectric material, wherein at least one of the first and second electrode comprises a diffusion barrier layer formed of  $\text{RuSi}_x$  using chemical vapor deposition, where x is in the range of about 0.01 to about 10.

B4  
34. (Once Amended) The structure of claim 32, wherein the first electrode comprises a diffusion barrier layer, wherein the diffusion barrier layer of the first electrode is formed on at least a portion of a silicon containing region, and further wherein the first electrode comprises one or more additional conductive layers formed over the diffusion barrier layer, the one or more additional conductive layers formed of at least one of a metal and a conductive metal oxide.

SW D3  
B5  
36. (Once Amended) A integrated circuit structure comprising:  
a substrate assembly including at least one active device and a silicon containing region;  
and  
an interconnect formed relative to the at least one active device and the silicon containing region, the interconnect including a diffusion barrier layer on at least a portion of the silicon containing region, wherein the diffusion barrier layer is formed of  $\text{RuSi}_x$  using chemical vapor deposition, where x is in the range of about 0.01 to about 10.